

Small-Form-Factor Optical Phased Array Module for Technology Adoption in Custom Applications

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Abstract: We present a small-form-factor optical phased array module with a 512-element array, driving CMOS ASICs, and interfacing FPGA. This $80 \times 40 \times 20 \text{ mm}^3$ module enables unprecedented evaluation and adoption of optical phased array technology for custom applications. © 2019 The Author(s)

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1. Introduction

Optical phased arrays (OPAs) are of great interest for a variety of applications requiring solid-state beam steering such as light detection and ranging (LiDAR) and free-space optical communication. Whereas OPA technology is rapidly maturing with increasingly complex demonstrations [1–6], wide-spread adoption of the technology has been limited by procuring and controlling these complicated integrated photonic circuits (PICs). Specifically, high power consumption, large form factors, and needed equipment to drive hundreds of elements has limited OPA use mainly to specialized laboratories. This has hindered OPA technology adoption outside of the integrated photonics community for the benefit of custom applications in numerous academic fields along with commercial sectors.

In this work, we present an OPA module for 2D solid-state beam steering containing a 512-element OPA, CMOS ASIC DAC banks, and an interfacing FPGA all within an $80 \text{ mm} \times 40 \text{ mm} \times 20 \text{ mm}$ form-factor. User operation only requires input electrical power ($\sim 4.9 \text{ W}$ total) and laser light through an epoxied fiber. Dynamic control is achieved with simple USB serial commands parsed by advanced FPGA firmware which holds pre-installed phase shifter look-up-tables (LUT) for beam steering. A point-to-point $8 \mu\text{s}$ steering time and $2 \mu\text{s}$ 10-90% settling time are achieved, a full-width at half-maximum (FWHM) beam diffraction angle of $0.04^\circ \times 0.02^\circ$ is demonstrated, and over 10,000 non-aliased resolvable beams are directly measured. The record-small form-factor and ease of use enables OPA evaluation by non-specialized users within their applications and brings a new era for the adoption of OPA technology.

2. Optical Phased Array Module Architecture

A block diagram of the OPA module is shown in Fig. 1(a) and a photograph of the front side is shown in Fig. 1(b). The module contains a high-density printed circuit board (PCB) with die-attached and wirebonded one-dimensional 512-element OPA (similar to [1] and [2]) and ASICs. Each of the three ASICs have ~ 171 DAC outputs routed to a respective phase shifter on the OPA (512 total). Laser light is input through an epoxied PM fiber and 2D beam steering is achieved by altering the phase shifters and input wavelength (no phase shifters voltage changes are necessary when varying wavelength). A system on module (SOM) FPGA is placed on the backside of the PCB, which parses USB serial commands and drives the ASIC digital inputs. The FPGA flash memory and external DDR SDRAM are used to store pre-installed OPA phase shifter calibration and LUTs for beam steering. The custom FPGA firmware enables scanning through a desired arbitrary sequence of LUT rows. The scan rate is user controlled and fundamentally limited by the FPGA logic and ASIC DAC rise/fall times. Additionally, individual phase shifters can be controlled for complex wavefront emission patterns for applications such as holography and optical trapping.

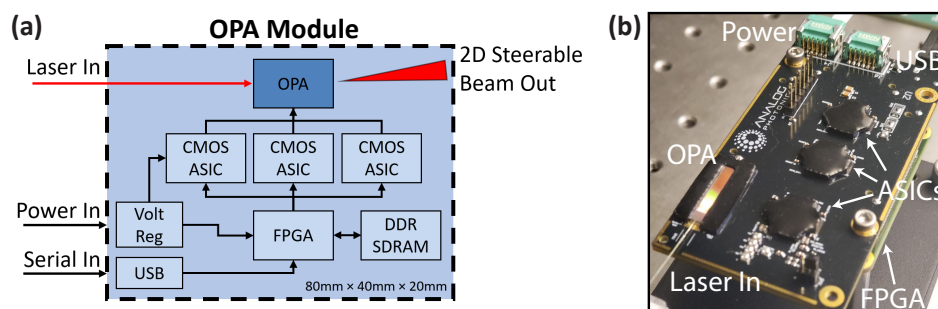


Fig. 1. (a) Block diagram of optical phased array module containing OPA, driving CMOS ASICs, and controlling FPGA on a $80 \text{ mm} \times 40 \text{ mm} \times 20 \text{ mm}$ module. (b) Photograph of module with major components labeled.

3. Optical Phased Array Module Measurements

Figure 2(a) shows the far field of the main beam before and after calibration of the element phase shifters. Due to the multi-millimeter-scale aperture, a small FWHM diffraction angle of $0.04^\circ \times 0.02^\circ$ is observed. Figure 2(b) plots the cross-section of the far field in the phase-controlled (θ) dimension where a side-lobe suppression of 12.3 dB is measured (13.3 dB theoretical), showing a high-fidelity calibration algorithm and phase shifter yield. To test the scan rate of the module, scanning was performed between two LUT rows and an external photodetector detected one of the beams. Figure 2(c) shows the output of the photodetector, where a record point-to-point period of $8\ \mu\text{s}$ was achieved, limited by the FPGA logic, and 10-90% settling time of $2\ \mu\text{s}$, limited by the ASIC rise/fall time constants. Figure 2(d) displays a 60×50 grid ($\theta \times \phi$) of summed far field spots while performing 2D beam steering with the phase shifters and input wavelength (1460 nm to 1610 nm). A non-aliased steering range of $22^\circ \times 20^\circ$ ($\theta \times \phi$) is shown in this measurement. Due to the small diffraction angle of the beam, the density of the grid was increased further and Fig. 2(e) shows a 110×100 grid. This measurement directly shows over 10,000 non-aliased points, to the best of our knowledge an experimental first for optical phased arrays. Theoretically, the module supports $>100,000$ resolvable points. The 512 phase shifters consume a total power of $<1\ \text{mW}$, independent of beam angle, the majority of module power consumption comes from the FPGA and ASICs (4.9 W).

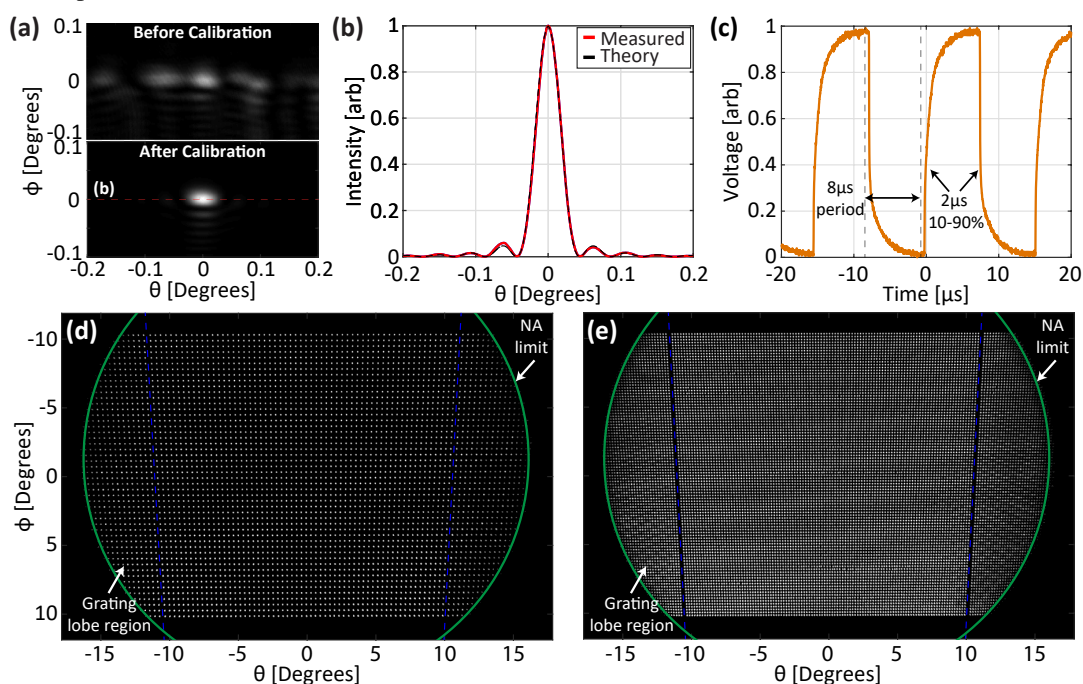


Fig. 2. (a) Far field profile before and after calibration. (b) Cross-section of far field in the θ dimension. (c) External photodetector output while performing beam steering showing a $8\ \mu\text{s}$ period and 10-90% settling time of $2\ \mu\text{s}$. (d) Sum of far field spots showing 2D beam steering on a non-aliased 60×50 and (e) 110×100 grid.

In conclusion, we have demonstrated a small-form-factor optical phased array module with a 512-element optical phased array, driving CMOS ASICs, and an interfacing FPGA. Whereas previous OPA demonstrations have mainly been limited to labs with bulky operating equipment, here the record-small form-factor and ease of use enables wide-spread evaluation and adoption of optical phased array technology. The high performance of the module with small diffraction angles ($0.04^\circ \times 0.02^\circ$ and $>10,000$ points), high-speed beam steering ($8\ \mu\text{s}$), and low-power operation ($\sim 4.9\ \text{W}$) enables numerous custom applications including LiDAR, data communication, holography, and trapping.

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References

1. C. V. Poulton, *et al.*, "High-Performance Integrated Optical Phased Arrays for Chip..." in CLEO 2018, paper ATu3R.2.
2. C. V. Poulton, *et al.*, "Optical Phased Arrays for Integrated Beam Steering," in GFP 2018, paper WC3.
3. S. A. Miller, *et al.*, "512-Element Actively Steered Silicon Phased Array for Low Power..." in CLEO 2018, paper JTh5C.2.
4. C. T. Phare, *et al.*, "Silicon Optical Phased Array with High-Efficiency Beam Formation over..." arXiv:1802.04624 (2018).
5. S. Chung, *et al.*, "A Monolithically Integrated Large-Scale Optical Phased Array in..." in IEEE JSSC, **53**, 275 (2018).
6. J. Notaros, *et al.*, "CMOS-Compatible Optical Phased Arrays with Monolithically..." in CLEO 2018, paper STu4B.2.